DISCONTINUOUS DIELECTRIC INTERFACE FOR BIPOLAR TRANSISTORS

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FIELD OF THE INVENTION

The present invention relates to a boundary layer to be formed between two regions of a semiconductor device structure. In particular, the present invention relates to a semiconductor device structure that includes at least one region of dielectric material between two regions of semiconductor material. The present invention also relates to process for forming such structures.

BACKGROUND OF THE INVENTION

Fig. 1 illustrates an example of a NPN bipolar transistor. The transistor illustrated in Fig. 1 includes a contact 1. The contact 1 may be made of a semiconductor material, such as polycrystalline silicon.

The contact 1 is formed over a region of a substrate 3 at a location where an emitter 5 of the transistor has been

formed. A layer 7 of a dielectric material may be arranged on the substrate between the emitter 5 and the contact 1. Often, the dielectric material of the layer 7 is an oxide.

Below emitter 5 lies the base region 9 of the transistor. Below region 9 lies collector 11. Fig. 1 also illustrates the doping and flow of current within an NPN bipolar transistor.

Under normal bias conditions, or forward active mode, the emitter-base (E-B) junction is forward biased, 5 and 9 in Fig. 1, and the collector base junction, 11 and 9 in Fig. 1. is reversed biased. Electrons are ejected from the emitter into the base. Then, the electrons diffuse across the base region where they are swept across the reverse biased C-B junction into the collector. The collector current I_C is associated with the flows of electrons from the emitter. On the other hand, the base current I_B is a function of the holes ejected from the base region. The holes can either recombine in the single crystal emitter or flow into the polysilicon emitter region 1, which is usually highly doped polycrystalline silicon.

The current again, beta (ß), may be described by the

relationship between the collector current and base current. Beta is defined as (collector current)/(base current). In other words, beta equals I_C/I_B. Generally, the desired value of beta is 100.

Resistance created by dielectric material of region 7 may affect the base current, as shown in Fig. 2. Along these lines, as the resistance created by the region between the contact 1 and the emitter 5 increases, base current decreases and, thus, beta increases. In contrast, if the resistance of region 7 is low, the resulting base current is high and, thus, beta is low.

Controlling the dielectric thickness in region 7 for a bipolar transistor typically is critical to controlling the current gain, beta.

Typically, two processes have been used for depositing polycrystalline (polysilicon) on the emitter Si in the past. According to the first process, a horizontal CVD polysilicon deposition tube has been used extensively. The polysilicon is deposited on the single crystalline Si emitter after the single crystalline Si has been precleaned. In this case, dielectric region 7 may be thin since the only oxidation

that occurs in region 7 in the transistor illustrated in Figs. 1 and 2 is that which occurs as the wafers enter the horizontal CVD tube. In this case, residual oxygen trapped in the system when the wafers are loaded may react with the emitter Si at insert temperatures of approximately 625°C. It has been found that very little oxidation of the emitter Si occurs in this instance. The resulting polysilicon is deposited on a Si surface with essentially native oxide.

Region 7 in this case has a very low resistance and, thus, Beta is low at approximately 50-60. Because the interfacial oxidation is essentially uncontrolled, Beta is found to be highly variable from lot to lot using the horizontal polysilicon deposition process.

In the second type of known process used, the polysilicon layer over the emitter may be deposited using a vertical chemical vapor deposition (CVD) polysilicon deposition tube in which the Si region of the emitter may be oxidized in situ, typically after an initial wet preclean. In this case, a batch of wafers may be loaded into the furnace, the chamber evacuated and then a mixture of an inert gas and oxygen may be leaked into the chamber at temperatures of approximately 600°C. In this case, Beta can

be set to 100.

However, different technologies of Bipolar transistors typically require different levels of interfacial oxide and, thus, need to be run separately. Also, variation of the level of oxidation across a batch of wafers can occur. In addition, the typical cost issues associated with batch versus single wafer processing are encountered.

SUMMARY OF THE INVENTION

The present invention addresses these and other problems by providing a process for forming at least one interface region between two regions of semiconductor material. The process includes forming at least one region of dielectric material comprising nitrogen in the vicinity of at least a portion of a boundary between the two regions of semiconductor material, thereby controlling electrical resistance at the interface.

Additionally, the present invention provides semiconductor devices prepared according to the above process.

Furthermore, the present invention provides a semiconductor device including a region of a first semiconductor material, and a region of a second semiconductor material. An interface region including at least one region of at least one dielectric material comprising of nitrogen is arranged in the vicinity of at least a portion of the boundary between the first region of semiconductor material and the second region of semiconductor material thereby controlling electrical resistance at the interface.

Still other objects and advantages of the present invention will become readily apparent by those skilled in the art from the following detailed description, wherein it is shown and described only the preferred embodiments of the invention, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned objects and advantages of the present invention will be more clearly understood when considered in conjunction with the accompanying drawings, in which:

Fig. 1 represents a cross-sectional view of a NPN bipolar transistor;

Fig. 2 represents a combined schematic and cross-sectional view of the embodiment of the transistor illustrated in Fig. 1;

Fig. 3a represents a cross-sectional view of a portion of an embodiment of a semiconductor device structure according to the present invention; and

Fig. 3b represents a close-up cross sectional view of a portion of the embodiment of a semiconductor device according to the present invention as illustrated in Fig. 3a.

DETAILED DESCRIPTION OF THE INVENTION

In order to control the base current and, thus, beta value of a polycrystalline silicon emitter based bipolar transistor, resistance at the interface between the polycrystalline silicon emitter and monocrystalline silicon substrate typically must be tightly controlled. The present invention controls base current, beta, and resistance through at least one region of dielectric material between the polycrystalline silicon emitter and the monocrystalline substrate. The dielectric material according to the present invention typically includes nitrogen. As described in greater detail below, the nitrogen may take a variety of forms.

In fact, the present invention is not limited to use at a boundary between monocrystalline and polycrystalline silicon. In fact, the present invention may be utilized at any interface between two regions of semiconductor material. The two regions of semiconductor material could include monocrystalline silicon, polycrystalline silicon, and/or amorphous silicon.

Examples of applications of the present invention

include BiCMOS devices (bipolar transistors and FET devices on the same chip). Along these lines the present invention may be utilized with heterojunction and homojunction bipolar transistors, DRAM cells, and any semiconductor device structure that includes amorphous silicon or polycrystalline silicon or SiGe or other materials are deposited on monocrystalline silicon or SiGe.

As stated above, the dielectric material between the two regions of a semiconductor material typically includes nitrogen. The nitrogen may be in any form. For example, the nitrogen could be in the form of implanted N+ or deposited N from a gaseous environment containing N_2O, NH_3, and/or NO forming Si_xN_y (a silicon nitride) and/or $Si_xO_yN_z$ (a silicon oxynitride).

The thickness of the nitrogen containing dielectric region(s) as well as the percentage of the boundary between the two regions of semiconductor material that the region(s) of dielectric material covers may vary depending upon the embodiment. Typically, the thickness and extent of the dielectric region(s) may depend upon the desired base current, resistance, and/or beta value it is desired that the final structure have.

According to the present invention, the dielectric region(s) may have a thickness of from about 1Å to about 10Å. The thickness may be measured with an elipsometer. The thickness may be in addition to native oxide film also measured with an elipsometer. Described in other terms, the dielectric material may be film having a thickness of less than one monolayer to a plurality of monolayers. A thickness of less than one monolayer indicates that the film does not entirely cover the boundary between the regions of semiconductor material.

The dielectric material could also be arranged in a single monolayer that covers the entire boundary between the two regions of semiconductor material. Some embodiments may include a plurality of monolayers. According to such an embodiment, regions may exist where no dielectric material is deposited between the regions of semiconductor material while in other regions, a plurality of layers of semiconductor material may be arranged between the regions of semiconductor material. Also according to such embodiments, some regions of the dielectric material may include a plurality layers while other regions include a fewer or greater layers of dielectric material.

The dielectric material may also include at least one oxide. Along these lines, references made to U.S. Patent Application Serial No. 09/165,946 for "beta control using a rapid thermal oxidation", the entire contents of the disclosure which is hereby incorporated by reference.

Fig. ~~1a~~ illustrates an example of a structure that the present invention may be utilized with. Fig. ~~1a~~ illustrates a region of monocrystalline silicon 1, a region of polycrystalline silicon 3 and an interface 5 between the region of monocrystalline silicon and polycrystalline silicon.

Fig. ~~1b~~ illustrates a close-up cross sectional view of a portion of the structure illustrated in Fig. ~~1a~~ including a plurality of regions of dielectric material between the two regions of semiconductor material. As such, Fig. ~~1b~~ illustrates a portion of a structure showing an example of an embodiment of the structure according to the present invention. Along these lines, Fig. ~~1b~~ illustrates a boundary region 7 including a plurality of regions 9 of dielectric material between the region of monocrystalline silicon 1 and the region of polycrystalline silicon 3. Arrows ~~11~~ represent current flowing between the regions of

semiconductor material.

According to one embodiment of the present invention, the at least one region of dielectric material is arranged on a sidewall of a trench formed in a monocrystalline silicon substrate. The trench is filled with non-monocrystalline silicon. Typically, the trench is filled with polycrystalline silicon or amorphous silicon in which some crystallization has taken place.

The placement of the region(s) of dielectric material relative to the interface region may depend upon the environment as well as the method utilized for creating the region(s) of dielectric material. According to one embodiment, the atoms or molecules of dielectric material may be implanted within one of the regions of semiconductor material. In other words, the atoms or molecules of dielectric material may be implanted within one or both of the regions of semiconductor material.

The atoms and/or molecules may be implanted under the surface of one or both of the regions of semiconductor material or at the surface of one or more of the regions of semiconductor material. According to one example, the

dielectric material includes nitrogen atoms implanted in the monocrystalline silicon. According to other embodiments, the dielectric material is deposited on a surface of one of the regions of semiconductor material, such as the monocrystalline silicon discussed above.

After forming the region(s) of dielectric material, the other region of semiconductor material may then be deposited or formed on the monocrystalline substrate and the dielectric region(s).

The present invention also includes processes for forming at least one interface region between two regions of semiconductor material. The method includes forming at least one region of dielectric material including nitrogen in the vicinity of at least a portion of a boundary between two regions of semiconductor material. The at least one region of dielectric material may be formed in a variety of ways.

According to one example, the at least one region of the dielectric material may be formed by implanting the dielectric material in the vicinity of the surface of one of the regions of semiconductor material. The dielectric

material may be implanted in one region of dielectric material prior to formation of the other region of semiconductor material.

According to one example, the dielectric material is created by implanting low doses of the dielectric material. Low doses may be desirable to help ensure that a discontinuous layer of dielectric is formed to result in the desired control of base current. According to one example, low levels of nitrogen are implanted.

The energy with which the nitrogen or other material(s) is implanted may be low enough such that the material(s) is/are not implanted to deep in the semiconductor material. According to one example, in which low levels of nitrogen are implanted in the dielectric material, the nitrogen is implanted at energies less than about 2 KeV. Typical implant energies may be in a range of about 0.1 KeV to about 5 KeV. The dosages of nitrogen utilized in this example may be in a range of from 1×10^{11} to 1×10^{14}.

After implanting the dielectric, an additional anneal process may be performed. The anneal process may be desirable to supplement the implantation process. For

example, some hot processes may not be adequate to form the discontinuous Si-N layer near the surface of the monocrystalline silicon.

According to one example, the anneal process may be a rapid thermal anneal. A rapid thermal anneal may be carried out at a temperature of about 900° C to about 1100° C for a time of about 1 second to about 60 seconds. Such a rapid thermal anneal may be used to form Si_xN_y (a silicon nitride) and/or $Si_xN_yO_z$ (a silicon oxynitride).

An advantage of implanting the dielectric material as described above is that photomasks may be utilized for tailoring implant conditions by region or device. On the other hand, a blanket film could be implanted in a region of semiconductor material. Residual dielectric may be removed after deposition and etching of the second layer of semiconductor material. For example, nitrogen could be implanted in the monocrystalline silicon as a blanket film. A residual material could be removed postpoly-Si deposition and etch.

According to a second example of a method according to the present invention for forming the region(s) of

dielectric material, one of the regions of semiconductor material may be subjected to elevated temperatures and a nitrogen-containing gaseous atmosphere. The gaseous atmosphere could include at least one N_2O, NO, and/or NH_3 gases. The temperature that the process may be carried out at could be anywhere from about 300°C to about 1,000°C. The semiconductor may be exposed to these temperatures and gases for a time period of about 1 to about 60 seconds.

Exposing a monocrystalline substrate to such an atmosphere and such a temperature for such a time, creates a discontinuous film on the surface of the monocrystalline silicon. The film may include silicon nitride and/or silicon oxynitride. However, the composition of the film may depend upon the nitrogen containing gas utilized in during the process as well as the temperature and time period that the process is carried out for.

The dielectric material created and the characteristics of the film created may also depend upon the semiconductor material that is exposed to the process of the invention. If the semiconductor material is monocrystalline silicon, then the dielectric material may be silicon nitride or silicon oxynitride if exposed to the above gases at the

above process parameters.

If the semiconductor material exposed to this second embodiment of a process according to the present invention for forming a dielectric layer is monocrystalline silicon, the process may be carried out after cleaning. The cleaning may be a wet process, plasma process, or reducing hot process.

Regardless of the material that the process is carried out on and the process materials, the process for carrying out the formation of the dielectric layer may be a rapid thermal process, fast thermal process (FTP), or conventual furnace process. A rapid thermal process typically is a rapid process carried out with quartz lamps. A fast thermal process typically is a small batch process that utilizing a conventional furnace. A conventional furnace typically utilizes a quartz tube with a ceramic cover and is heated resistively.

During this second example of a process according to the present invention, the substrate may be exposed to the elevated temperatures according to a variety of regimens. For example, the substrate may be exposed to the full

elevated temperature immediately. Alternatively, the temperature that the substrate is exposed to may be ramped up over a period of time.

According to one example, the temperature that the substrate is exposed to is ramped up at a rate of about 75° C per second to a temperature of about 400° C to about 800° C. The rate that the temperature may be ramped up may be about 5° C per second to about 100° C per second.

According to the example in which the temperature is ramped up at a rate of about 75° C per second, ammonia gas may flow into the container that the process is being carried out in at a rate of about 5 standard liters per minute (SLPM) for a time of about 5 seconds to about 15 seconds.

After exposing the substrate to elevated temperatures, regardless of whether the temperatures are ramped and the final temperature, the substrate may then be cooled. The substrate may be cooled actively or passively. Along these lines, the process may include some intervention for increasing the rate of cooling beyond what would be experienced in simple convection of heat from the substrate.

According to one example, the substrate is cooled at a rate of about 15° C to about 30° C per second.

After cooling, the substrate may be extracted from a processing chamber or other space where the process is carried out.

The process according to the second example may result in a dielectric layer having a thickness of about 1Å to about 10Å, when measured elipsometrically. However, process parameters may be controlled to produce dielectric layer or layers of any desired thickness and percentage of area coverage of the boundary between the two regions of semiconductor material.

After forming the dielectric region(s) through exposure to temperatures and nitrogen containing gas, the second region of semiconductor material may be provided on the first region of semiconductor material and the dielectric region(s). The dielectric region(s) may remain through deposition of the second region of semiconductor material. Any residual dielectric material or any dielectric material that is desired to be removed may be removed after or during etch of the second region of semiconductor material.

A third example of a process according to the present invention may be utilized for forming a dielectric region in the vicinity of a boundary between two regions of semiconductor material includes a very thin chemical vapor deposition process. The chemical vapor deposition process may vary from embodiment to embodiment. According to one embodiment, a low pressure chemical vapor deposition process (LPCVD) may be utilized. Another embodiment utilizes a plasma enhanced chemical vapor deposition (PECVD) process.

Regardless of the chemical vapor deposition process utilized, this third example of a process for creating a region(s) of dielectric material may be utilized to create a discontinuous film on one of the regions of semiconductor material. For example, the chemical vapor deposition process may be utilized to create a discontinuous film on monocrystalline silicon that may serve as an emitter in a semiconductor device.

The chemical vapor deposition process may utilize a silicon source gas. One example of a silicon source gas that may be utilized with a CVD process according to the third example of the present invention is silane and/or dichlorosilane (DCS). Other silicon source gases may also

be utilized in a chemical vapor deposition process.

The chemical vapor deposition process may also utilize a nitrogen/oxygen source gas. The nitrogen/oxygen source gas may vary, depending upon the embodiment. Examples of nitrogen/oxygen source gases may include NH_3 and N_2O.

If both oxygen and silicon source gases are utilized in the CVD process, the ratio of silicon source gas to nitrogen/oxygen source gas may vary to achieve a desired silicon-nitrogen/oxygen stoichiometry. The flow and ratio of these gases may also vary depending upon the characteristics of the layer or layers of dielectric material that it is desired to create.

The ratio of gases in the CVD processes may be controlled to utilize various ratio proportions to produce voids.

The process parameters of the chemical vapor deposition process utilized may vary depending upon, among other things, the desired characteristics of the dielectric region(s) that is desired to create and the gases that are being utilized. Typically, the chemical vapor deposition

process is carried out at a temperature of about 600°C to about 800°C. The gas flow may also vary depending upon the embodiment. Typically, the deposition gases may flow for a time less than about 5 seconds.

A chemical vapor deposition process such as described herein may be utilized to create a film of a thickness with less than one monolayer. The film may have a thickness of about 1 to about 10Å.

As stated above, regardless of the process utilized for creating the dielectric region(s), the dielectric material may be deposited on a sidewall of trench formed in a monocrystalline silicon substrate, with the trench subsequently being filled with polycrystalline silicon.

The dielectric region(s) may also include at least one oxide as also described above.

The present invention also includes a device prepared by a process such as the process described above.

Advantages of the present invention include that by utilizing implantation, the present invention may allow

tailoring of beta by specific region or device. Additionally, an oxynitride interfacial dielectric may be more robust with subsequent thermal processing in a DRAM structure. Furthermore, a nitride-containing dielectric region may not be consumable by subsequent hot processes. The present invention also allows a high degree of control of NPN-ß in polysilicon emitters. A nitrogen containing dielectric region(s) also help reduce retention defects in trench DRAM buried strap processes.

The present invention may also include a rapid thermal anneal (RTA) when an N implant is utilized to form an Si-N species. The rapid thermal anneal is described above in greater detail.

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention, but as aforementioned, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings, and/or the skill or knowledge of

the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.